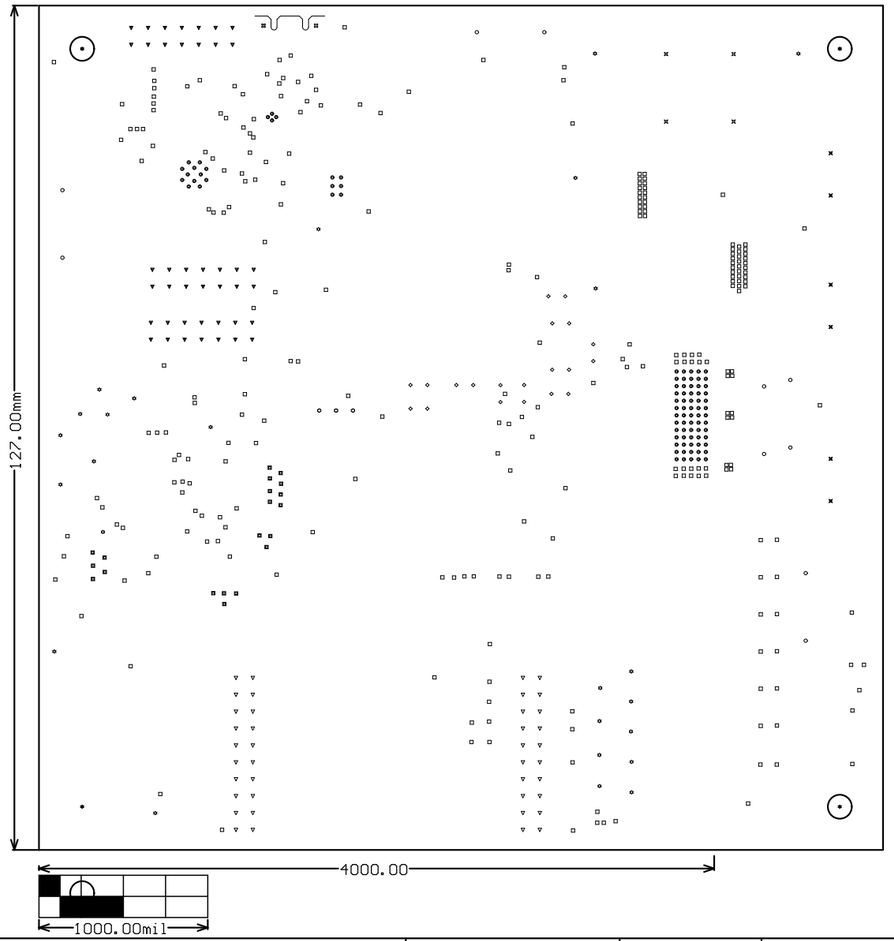
Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
◎	87	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
□	263	13.78mil (0.350mm)	PTH	Round	Top Layer - Bottom Layer	
▣	20	17.72mil (0.450mm)	PTH	Round	Top Layer - Bottom Layer	
◇	20	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
▽	40	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	
▼	42	43.31mil (1.100mm)	PTH	Round	Top Layer - Bottom Layer	+/-1.97mil
⌬	3	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	
○	10	51.18mil (1.300mm)	PTH	Round	Top Layer - Bottom Layer	
✖	6	59.06mil (1.500mm)	PTH	Round	Top Layer - Bottom Layer	
⌘	4	62.99mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
☼	25	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
✱	4	141.73mil (3.600mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	2	23.62mil (0.600mm)	PTH	Slot	Top Layer - Bottom Layer	
	526 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		2.80mil		
	Dielectric 1	FR4 370	11.40mil	4.2	
2	Signal Layer 1		1.40mil		
	Dielectric 2	FR4 370	30.00mil	4.2	
3	Signal Layer 2		1.40mil		
	Dielectric 3	FR4 370	11.40mil	4.2	
4	Bottom Layer		2.80mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER _____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER _____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE:	DRV8452EVM
DESIGNED FOR:	Public Release
FILE NAME:	MD040_RevA.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: MD040	REV: A	SVN REV: 40a3f0cfbcc7abc6bcb2404f1f24a5fc731ee022 [Locally Modified]
LAYER NAME = [illegible]ions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 1/4/2023 11:59:15 AM	TEXAS INSTRUMENTS	

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ENGINEER: Pedro Arango Ramirez	LAYOUT BY: .PCB_Layout
SCALE: 1.12	ALTIUM DESIGNER VERSION: 23.0.1.38